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| 09/927,425 | 08/10/2001 | Brian J. Kaczynski | 73169/278153<br>ATH-030(U) | 6391 |

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MCLEAN, VA 22102

| EXAMINER | |
|---|---|
| TORRES, JUAN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2631 | |

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/927,425 | KACZYNSKI, BRIAN J. | |
| | Examiner | Art Unit | |
| | Juan A. Torres | 2631 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-23* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Claims 1-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **with** traverse in the reply to the first Office Action on 03/24/2005.

### *Drawings*

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **OUTN and OUTP** (page 14 line 7 of the disclosure); **OUTN and OUTP** (page 14 line 8 of the disclosure). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

In view of the amendment filed on 03/24/2005, the Examiner withdraws claim objections of claims 4, 26 and 29 of the previous Office Action.

***Response to Arguments***

Applicant's arguments filed on 03/24/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Regarding claim 24, Jett fails lo disclose or suggest the elements as alleged in the Office Action. For example, the Examiner alleges that Jett discloses a variable gain amplifier including an inductively loaded folded cascode circuit that inputs an input differential signal having a referenced output level and outputs a current, as required by claim 24. However a review of the cited figure 3 of Jett reveal that, while superficially similar, the Jett amplifier operates in a manner significantly different from amplifiers according to the presently claimed invention. Figure 3 of the present application illustrates the claimed current output (OUTP and OUTN of the present application), while figure 3 of Jett clearly shows a voltage output (21 and 21 ' of Jett and see also Jett at col. 3 lines 23-44)."

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the system presented by Jett will output a voltage and a current when connected (see column 1 lines 2-25).

The Applicant contends, "Further, the outputs from the Jett circuit (21 and 21 ' of Jett) correspond to the inputs to the inductively folded cascode circuit of the present invention (DN 113 and DP 115 of the present application)".

The Examiner disagrees and asserts, that, the system presented by Jeff is not the input of the circuit presented in the present invention.

The Applicant contends, "The differences in input and output configuration are relate to functional differences in application of le circuit of Jett and the present invention and demonstrate clearly that Jett does not disclose or otherwise suggest an inductively loaded folded cascode circuit that ... outputs a current" as required by claim 24. Because Jett does not disclose an essential element of claim 24, and the Office Action does not allege that this element is found in Vagher either, Applicant respectfully submits that claim 24 patentably defines over the Jett/Vagher combination for at least this reason".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the system presented by Jett in combination with the system presented by Vagher is not patentability different form the system presented in the present invention.

The Applicant contends, "The Examiner acknowledges that Jett fails to disclose remaining elements of claim 24 but suggests that Vagher discloses "a digitally switched gain amplifier with a plurality of gain cells each gain cell coupled to the input current load circuit and receiving the output differential signal..." Applicant respectfully disagrees. Vagher is directed to a high-gain adjustable chain of amplifier (see table 1 col. 4 line 45, showing gains on the other of 115 dB). The device disclose by Vagher are former from serially connected amplifiers for providing the desired high gain (see Vagher at figure 1 and col. 2, lines 37-44)".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action Vagher discloses a digitally switched gain amplifier with a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output

differential signal, each gain cell comprising two current mirror circuits (figure 3 blocks Q30/Q32 and Q34/Q36, column 4 lines 65-69). The following paragraph is taking from the mentioned patent: "FIG. 3 shows a schematic diagram for a four gain state amplifier cell such as $A_1$. This is an extension of the 2 state cell. The four pairs of transistors $Q_{20}$ and $Q_{25}$, $Q_{21}$ and $Q_{26}$, $Q_{22}$ and $Q_{27}$, and $Q_{23}$ and $Q_{28}$ are connected in parallel such that only one pair determines the gain"

The Applicant contends, "In contrast one of the objects of the present invention includes the provision of an apparatus and a method that allow for gradual step increases in output power to avoid the output power from exceeding a predetermined maximum output power and the provision of a method of operating a variable gain amplifier using the sensed output power to determine whether to back-off from the current output power. Embodiments of the invention achieve these and other objectives by providing, for example...multiple ones of the gain cells 160 in the variable gain amplifier 130 will be connected in parallel such that two signals, GN and GP, drive the common GN and GP input of all of the gain cells, and two outputs, OUTN and OUTP, will be driven by the common OUTN and OUTP outputs of all of the gain cells.

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the discussion is based only in the claim limitations.

The Applicant contends, "See the present specification at page 14, lines 5-9. It will be appreciated them that the parallel the parallel connected amplifiers of the present invention present an arrangement different from the serially connected amplifier of Vagher. Specially in contrast to Vagher and required by claim 24, in the present

invention each gain is couple to the input current load circuit and receives the output differential signal. Further, the objective of controlling output power below a maximum is starkly different from Vagher's objective of maximizing output power. Therefore the configuration and purpose of the present invention are substantially different from the configuration and purpose of the combine Jett and Vagher applications and the cited references cannot be said to anticipate or suggest the subject matter of the present invention".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action the discussion is based only in the claim limitations and FIG. 3 shows a schematic diagram for a four-gain state amplifier cell such as $A_1$. This is an extension of the 2 state cells. The four pairs of transistors $Q_{20}$ and $Q_{25}$, $Q_{21}$ and $Q_{26}$, $Q_{22}$ and $Q_{27}$, and $Q_{23}$ and $Q_{28}$ are connected in parallel such that only one pair determines the gain.

The Applicant contends, "Claim 24 further requires that each switched circuit (is) coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity of the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of the gain cells in the positive mode than in the negative model. Vagher does not disclose or suggest these very specific claim limitations. Col. 4, lines 60-64 relied on the Office Action merely disclose the operation of one amplifier (i.e. the alleged gain cell) to set a gain value. This does not disclose or suggest anything about how the switching circuits operate, much less to place more of the plurality of gain cells in the positive mode than in the negative mode, " as required by claim 24.

The Examiner disagrees and asserts, that, as indicated in the previous Office Action Vagher discloses a digitally switched gain amplifier with a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits (figure 3 blocks $Q_{30}$/ $Q_{32}$ and $Q_{34}$/ $Q_{36}$, column 4 lines 65-69); and a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity to the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode (figure 3 blocks $Q_{20}$- $Q_{25}$, column 4 lines 60-64)

The Applicant contends, "Applicant observes that Tanji is directed to a variable gain amplifier and Yun is directed to smart antenna systems. Neither of these references is directly related to the transceiver having a constant power output of the present application. Therefore, Applicant respectfully summits that combination: Vagher, Jett, Yun and Tanji fail to disclose all elements of claims 25-33 or to render these latter claims obvious.

The Examiner disagrees and asserts, that, as indicated in the previous Office Action Tanji (US 6201443) discloses variable gain amplifier fabricated in complementary metal oxide semiconductor technology in which each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors, and Yun (US 6463295) discloses an intermediate frequency upmixer (figure 1 block 157, column 17 line 31) having a intermediate frequency upmixer output coupled to an input of the

variable gain amplifier (figure block 159, column 17 line 33); and a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier (figure 1 block 167, column 17 line 40).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24, 25, 26, 27, 30 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jett et al. (US 4520324), and further in view of Vagher (US 5313172).

As per claim 24 Jett discloses a variable gain amplifier including an inductively loaded folded cascode circuit that inputs an input differential signal having a referenced output level and outputs a current (figure 3 block 19, column 3 line 34); an input current load circuit that inputs the current from the inductively-loaded folded cascode circuit and outputs an output differential signal having a ground-referenced output level (figure 3 blocks 21 and 21', column 3 line 37). Jett doesn't disclose a plurality of gain cells and a plurality of switches. Vagher discloses a digitally switched gain amplifier with a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits (figure 3 blocks Q30/Q32 and Q34/Q36, column 4 lines 65-69); and a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative

mode having an opposite polarity to the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode (figure 3 blocks Q20-Q25, column 4 lines 60-64). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 24.

As per claim 25, Vagher and Jett teach claim 24, Vagher also discloses that a positive mode and the negative mode occur at the same time in a gain cell of the variable gain amplifier, thereby providing for fine gain adjustments (figure 3 blocks $+V_{IN}$ and $-V_{IN}$). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 25.

As per claim 26, Vagher and Jett teach claim 24, Jett also discloses an input current load circuit comprised of four NMOS transistors arranged in a cascode configuration (figure 3 blocks I3, I3', I2, and I2', column 3 line 38). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 26.

As per claim 27, Vagher and Jett teach claim 26. Vagher also discloses that Jett outputs 21 and 21' can be connected to the VCA1 and VCA2 of Vagher and the input current load circuit is mirrored by each of the plurality of gain cells (figure 3 column 4 line 60 to column 5 line 13). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 27.

As per claim 30, Vagher and Jett teach claim 24. Vagher also discloses that Jett outputs 21 and 21' can be connected to the VCA1 and VCA2 of Vagher and the input current load circuit is mirrored by each of the plurality of gain cells and the input current load circuit is mirrored by each of the plurality of gain cells (figure 3 column 4 line 60 to column 5 line 13). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 30.

As per claim 34, Vagher and Jett teach claim 24. Vagher also discloses that the input current load circuit is commonly connected to each gain cell and the gain cells have inputs for receiving the output differential signal, the inputs of each cell being commonly connected to the output differential signal (figure 3 column 4 line 60 to column 5 line 13). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched

gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 34.

As per claim 35, Vagher and Jett teach claim 24. Vagher also discloses that the switching circuits operate to place a selected portion of le plurality of gain cells in the positive mode, the portion being selected to maintain a preferred output power level (figure 3 column 4 line 60 to column 5 line 13). Jett and Vagher are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett the connection of the digitally switched gain amplifier with a plurality of gain cells disclosed by Vagher. The suggestion/motivation for doing so would have been to reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 35.

Claims 28-29 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vagher (US 5313172), in view of Jett et al. (US 4520324) and further in view of Tanji (US 6201443).

As per claim 28, Vagher and Jett teach claim 27. Vagher doesn't disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. Tanji discloses variable gain amplifier fabricated in complementary metal oxide semiconductor technology in which each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. Jett, Vagher and Tanji are analogous art because they are from the same field of endeavor. At the time

of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett and Vagher the variable gain amplifier fabricated in complementary metal oxide semiconductor technology disclosed by Tanji. The suggestion/motivation for doing so would have been to provide an inexpensive and well-known standard element and in order to reduce the power consumption of the digitally switched gain amplifier (Tanji column 2 lines 32-41). Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 28.

As per claim 29, Vagher, Jett and Tanji teach claim 28. Jett also teaches plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode (figure 3 column 3 lines 23-28). Jett, Vagher and Tanji are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett and Vagher the variable gain amplifier fabricated in complementary metal oxide semiconductor technology disclosed by Tanji. The suggestion/motivation for doing so would have been to provide an inexpensive and well-known standard element and in order to reduce the power consumption of the digitally switched gain amplifier (Tanji column 2 lines 32-41). Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 29.

As per claim 31, Vagher and Jett teach claim 24. Vagher also disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NPN bipolar transistors (figure 3 column 4 line 60 to column 5 line 13). Vagher doesn't disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. Tanji discloses variable gain amplifier fabricated in complementary metal oxide semiconductor technology in which each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors (figure 2 column 2 lines 42-64). Jett, Vagher and Tanji are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett and Vagher the variable gain amplifier fabricated in complementary metal oxide semiconductor technology disclosed by Tanji. The suggestion/motivation for doing so would have been to provide an inexpensive and well-known standard element and in order to reduce the power consumption of the digitally switched gain amplifier (Tanji column 2 lines 32-41). Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 31.

As per claim 32 Vagher and Jett teach claim 24. Jett also teaches a plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode (figure 3 column 3 lines 23-28). Jett, Vagher and Tanji are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain

amplifier disclosed by Jett and Vagher the variable gain amplifier fabricated in complementary metal oxide semiconductor technology disclosed by Tanji. The suggestion/motivation for doing so would have been to provide an inexpensive and well-known standard element and in order to reduce the power consumption of the digitally switched gain amplifier (Tanji column 2 lines 32-41). Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 32.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jett et al. (US 4520324) further in view of Vagher (US 5313172) and further in view of Yun (US 6463295). Jett and Vagher teach claim 24. Vagher and Jett don't disclose an intermediate frequency upmixer having a intermediate frequency upmixer output coupled to an input of the variable gain amplifier; and a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier. Yun discloses an intermediate frequency upmixer (figure 1 block 157, column 17 line 31) having a intermediate frequency upmixer output coupled to an input of the variable gain amplifier (figure block 159, column 17 line 33); and a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier (figure 1 block 167, column 17 line 40). Jett, Vagher and Yun are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the variable gain amplifier disclosed by Jett and Vagher in the transmitter chain described by Yun. The suggestion/motivation for doing so would have been to in order to provide an inexpensive and well-known standard element and in order to reduce the power

consumption of the variable gain amplifier disclosed by Yun. Therefore, it would have been obvious to combine Jett with Vagher to obtain the invention as specified in claim 33.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Khoury et al. (US 5867778) title "Switched gain element" discloses a switched gain element that has an input differential transistor pair and a gain control stage formed of a transistor quad. The four transistors of the transistor quad are connected through respective impedances to a supply voltage. The junction of the impedances and the transistors are connected through further respective transistors to output terminals. The further transistors are switched on by respective control voltages applied to switchable current sources. The same control voltages are applied to the transistor quad. Thus, when first predetermined voltages are applied a first voltage corresponding to the value of two of the impedances is output and when second predetermined voltages are applied a second voltage corresponding to the value of the remaining two impedances is output. The invention may also be applied to a mixer for switching the gain. Sessions (US 6154018 A) discloses a high differential impedance load device. Brunner (US 6046640 A) discloses a switched-gain cascode amplifier using loading network for gain control. Sahota (US 5880631 A) discloses a high dynamic range variable gain amplifier.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
04-25-2005

M. G/

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER

REPLACEMENT SHEET

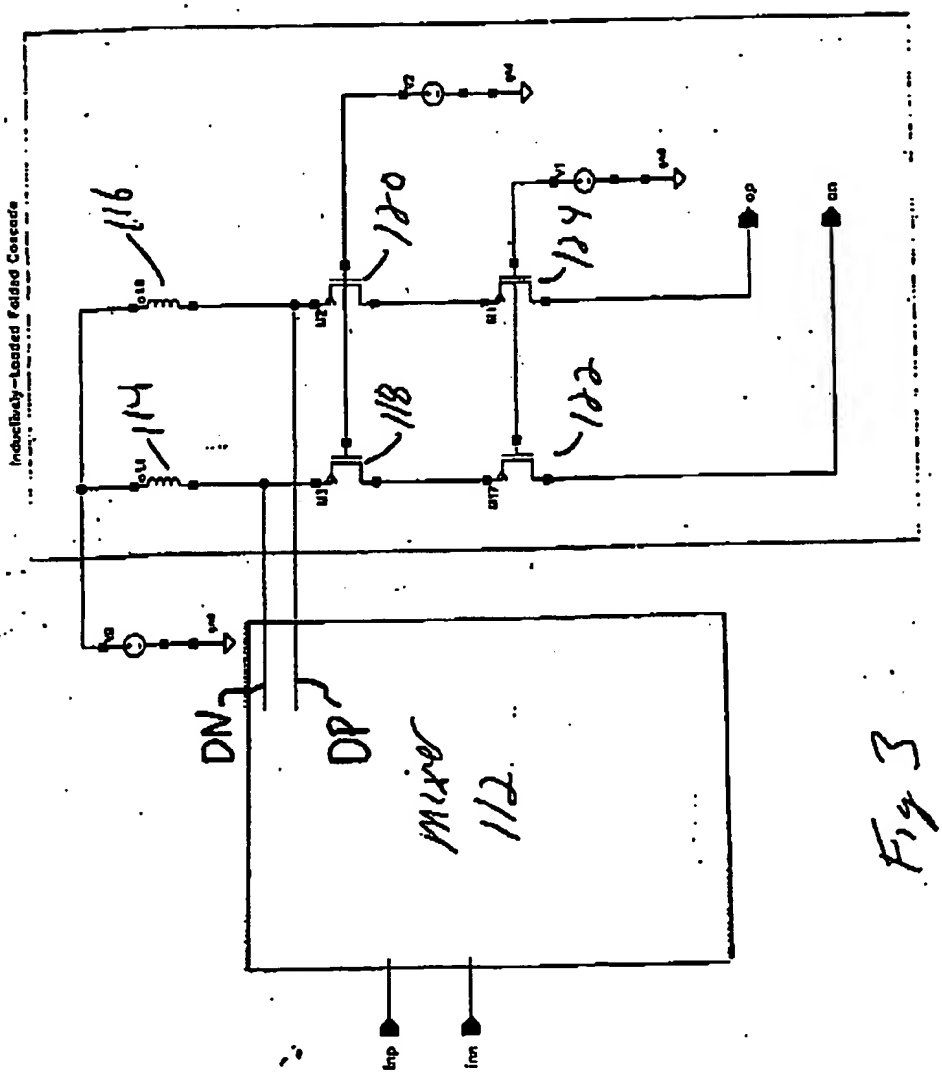


Fig 3

REPLACEMENT SHEET

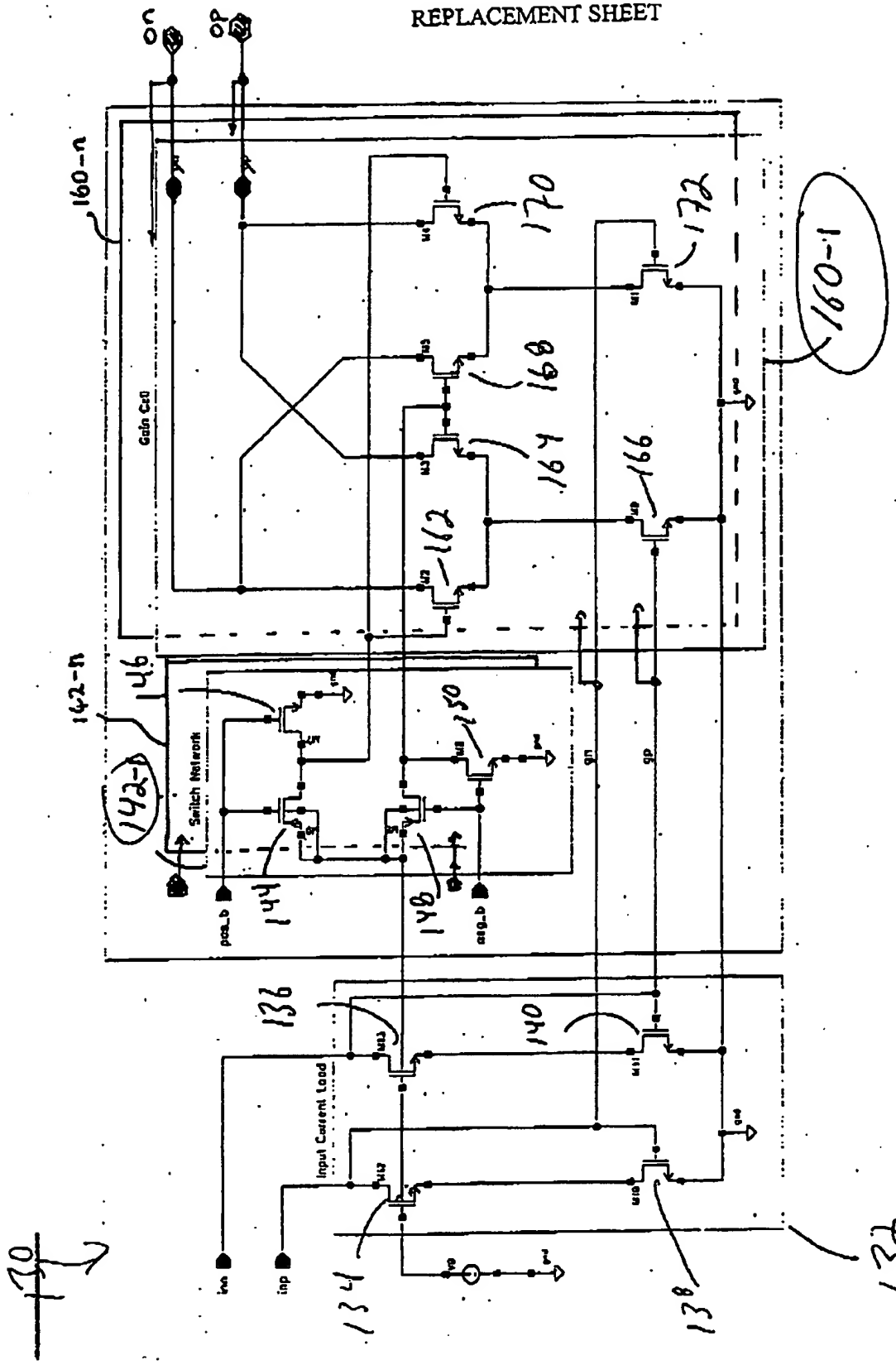


Fig 4

ANNOTATED SHEET

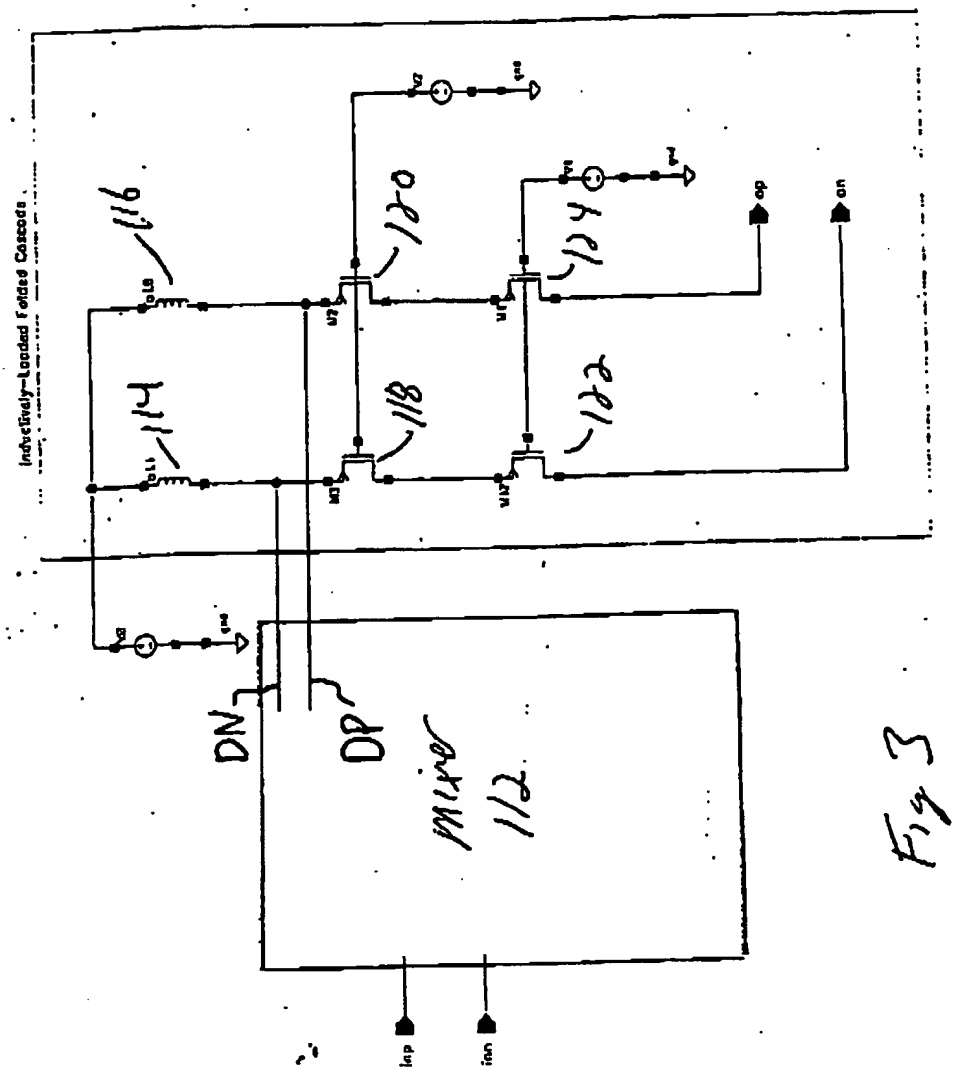


Fig 3

ANNOTATED SHEET

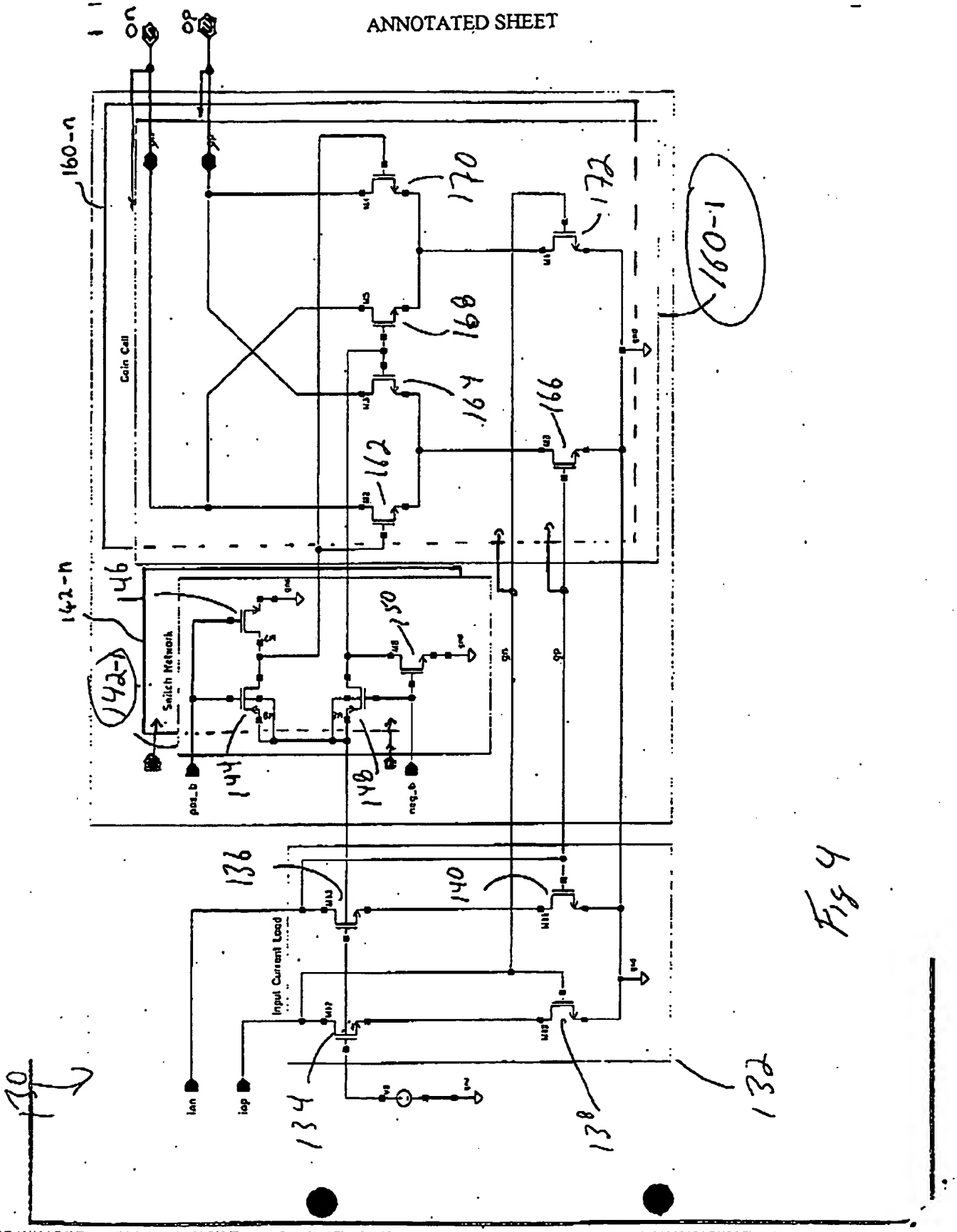


Fig 4